ABSTRACT OF THE DISCLOSURE

A memory circuit and method to improve signal margin is disclosed. The circuit includes a memory array arranged in rows 702, 704, 706 and columns 750, 752 of memory cells. Each row of memory cells is connected to a respective wordline. Each column of memory cells is connected to one of a bitline and a complementary bitline. An active wordline accesses a respective row of memory cells. The memory circuit includes a plurality of precharge circuits 724, 726, 728. Each precharge circuit is connected to a respective column of memory cells and coupled to receive a precharge signal PRE. An active precharge signal renders a respective precharge circuit conductive. A control and decode circuit 700 changes an inactive wordline signal to an active wordline signal while the precharge signal is active.